

## High Efficiency Single and Push-Pull Power Amplifiers

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## ABSTRACT

In this paper, a high efficiency single and push-pull power amplifiers are described. We can construct the high efficiency power amplifier by using the higher harmonics along with the fundamental wave. By connecting the parallel resonators for the fundamental wave  $f_0$  and the third harmonic  $3f_0$  to the load circuit of the amplifier, we can synthesize a square wave which is necessary for obtaining the efficiency amplifier. The single and push-pull power amplifiers were constructed and tested. The operating frequency was 0.9 GHz, and the maximum output power and the power added efficiency were 36.1 dBm and 60 %, respectively, for the single amplifier and they were 39 dBm and 81 % for the push-pull power amplifier.

## I. INTRODUCTION

In recent years, there is a strong demand that the efficiency of an amplifier for a transmitter used at a mobile station in the 0.6 to 2.4 GHz band should be made higher, and the studies related to this subject have been reported (1)-(4). In Refs.(1) and (2), the high efficiency was accomplished by short-circuiting the impedance of the output circuit of an amplifier for even harmonics. In Ref.(3), to construct a high efficiency amplifier, a short-ended  $\lambda/4$  transmission line or an open-ended transmission line was used in the load circuit. In Ref.(4), the efficiency of a second-harmonic processing circuit is maximized by the second-harmonic injection method.

In the above cited methods, the fundamental wave and the second harmonics are employed to construct a high efficiency amplifier. In these methods, we make the amplitude of a sinusoidal wave saturated at its maximum and uses this waveform as an exciting waveform, and the power added efficiency becomes large at a saturating point of the output power. Since we cannot use the amplifier at this saturating point even if the efficiency is high, we should use a point below the saturating point and, therefore, the power added efficiency is low. To overcome these problems, the author proposes the use of the fundamental and the third-harmonic waves and constructed single and push-pull amplifiers using these waves.

To obtain high efficiency, we set the amplitude of the third harmonics to a value in the range  $1/6 - 1/7$  when the amplitude of the fundamental wave is unity. If we set the operating angle of the synthesized voltage waveform to a value in the range  $70^\circ - 74^\circ$ , we can obtain a square waveform which is necessary for a high efficiency amplifier and can construct an amplifier with high power added efficiency.

The author constructed the class B single and push-pull power amplifiers and performed the experiment at

the operating frequency of 0.9 GHz. The output power was 36.1 dBm for the single amplifier and 39 dBm for the push-pull amplifier. The power added efficiencies were 60 % and 81 % for the two amplifiers. In the following sections, the characteristics of these amplifiers are described.

## II. HIGH EFFICIENCY POWER AMPLIFIER

## 2.1 High efficiency single power amplifier

As a power amplifier in a conventional transmitter, class C amplification is adopted where the drain efficiency of FET is high. In a drain circuit, we tune the frequency at a point where the power factor is unity, choose a deep gate bias, and give the exciting voltage which is large enough to have the plus gate voltage. Further, we make the current flow angle of the drain smaller than  $\pi$ . Figure 1 shows the drain voltage under these conditions. The current flow angle is an electrical angle corresponding to a time interval in which the drain current flows. The operating angle is a half of the current flow angle. The operating angles for class A, B, and C amplification are  $\pi$ ,  $\pi/2$ , and  $\pi/4$ , respectively.

When we use a FET in class C amplification, the drain efficiency is 75 - 82 % and a part of the input power is lost. If the drain voltage is zero in a period when the drain current flows, the loss is zero, and the efficiency is 100 %. In class C amplification, if we reduce the operating angle or the current flow angle  $2\theta_1$ , the drain voltage is low in a period when the drain current flows. As a result, the efficiency becomes high as shown in Fig. 1. However, if we want to have large power by making the operating angle small, both the drain current and drain voltage increase and the loss also increases. Hence, too small operating angle makes the efficiency lower.

When the input voltage to the gate of FET is a square wave, the drain current is a square wave. Since the drain current flows when the drain voltage is low, it is possible to make the efficiency of FET 90 - 95 %.

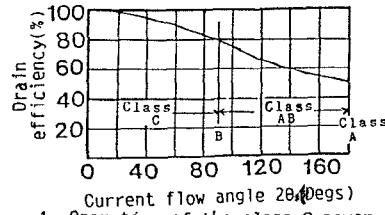


Fig. 1. Operation of the class C power amplifier relation between the current flow angle and the drain efficiency

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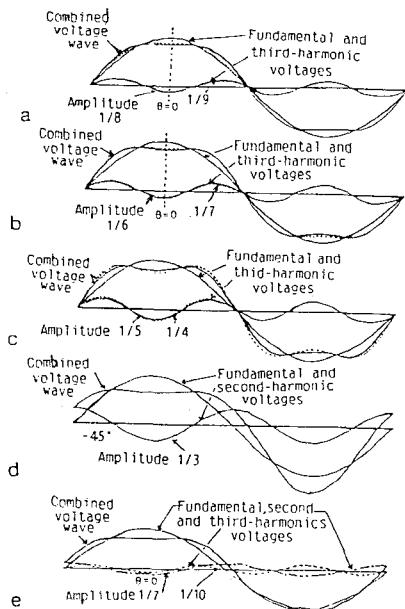


Fig. 2. Waveform of the voltage synthesized by the fundamental wave and the second harmonics, and the third harmonics

When we increase the amplitude of a sinusoidal wave given to the gate of FET, we have the fundamental wave and the second and third harmonics at the drain, because the characteristic curve of FET is nonlinear (we neglect the higher-order harmonics as their amplitudes are very small). By adjusting the ratio between the amplitude of the fundamental wave and that of the harmonics, we synthesize a voltage waveform. When this voltage is applied to the gate of the amplifier, the current flows in an interval when the drain voltage is low and, as a result, the power added efficiency is high. The synthesized voltage waveform is shown in Fig. 2. As indicated in Figs. 2a - 2c, we first choose the phase of the third harmonics so that the third harmonics is out of phase with respect to the fundamental wave at  $\theta = 0$ . Next we consider how the amplitude of the third harmonics should be chosen to obtain the waveform that is close to a square wave necessary for a high efficiency amplifier. Let us assume that the amplitude of the fundamental wave is unity. Then if we set the amplitude of the third harmonics to 1/8 or 1/9, the flat waveform is obtained at a point where the amplitude takes its maximum as shown in Fig. 2a. However, the width of the flat portion is narrow. Next if we set the amplitude of the third harmonic to 1/6 or 1/7, the flat portion is wider than that in Fig. 2a and the waveform is close to a square wave as shown in Fig. 2b. Further, if we set the amplitude to 1/4 or 1/5, the waveform has two peaks at its maximum as shown in Fig. 2c.

Now let us use the fundamental wave and the second harmonics that are shown in Fig. 2d. When the amplitude of the second harmonics is 1/3 and the phase retardation is 45°, the two waves become out of phase at  $\theta = 0$  and we obtain the maximally flat waveform that is close to a square wave. In a case where we use the fundamental wave and the second and third harmonics that are shown in Fig. 2e, we set the amplitudes of the second and third harmonics to 1/7 and 1/10, respectively, and we delay the phase angle of the second harmonics by 45°. Then the two harmonics become out of phase with respect to the fundamental wave and the synthesized wave has a flat portion at its maximum. As a result, we obtain a

square wave which is necessary for the high efficiency amplifier. The operating angle of this synthesized wave is slightly smaller than that of the wave obtained when the fundamental wave and the second harmonics are used. As evident from Figs. 2a - 2e, the synthesized wave that has small operating angle and is closest to a square wave is the wave shown in Fig. 2b. This wave has a wide flat portion, and if we use this wave at the exciting port of a power amplifier and at gate of an FET of the final stage, the period where the drain voltage is low becomes longer. It seems that, if the drain current flows in this period, we may obtain a high efficiency amplifier. However, the current flow angle  $2\theta$  becomes large and the efficiency decreases. Figure 1 shows how the drain efficiency depends on the angle  $2\theta$ . Note that this figure was obtained for a sinusoidal waveform and cannot be compared directly with the result obtained for the waveform in Fig. 2. But, as long as we judge from Fig. 1, it seems that the efficiency decreases as  $2\theta$  becomes large.

Although the waveform synthesized using the fundamental wave and the third harmonics has flat portion at its maximum, it spreads out a little at the foot and differs slightly from the desired waveform. As a result, the efficiency is smaller than that attainable for the optimum waveform. Then it becomes most important how we choose the operating angle to realize the high efficiency amplifier.

When the operating angle  $\theta_1$  of the synthesized waveform falls in the range 70° - 74°, the waveform is closest to a square wave. Therefore this range of the angle is desirable. The method for adjusting  $\theta_1$  to a value in this range is shown in Fig. 3. (The waveform is symmetrical with respect to  $\theta = 0$  and, if we choose 74° at either side of  $\theta = 0$ , we need only the waveform above the line.)

Figure 3 shows a circuit system for producing the synthesized voltage waveforms indicated in Fig. 2. When we increase the amplitude of voltage applied to the input of the first-stage amplifier, the second and third harmonics as well as the fundamental wave are generated at the drain because of the nonlinear characteristics of an FET. As shown in Fig. 2, we connect the filter which transmits only the fundamental wave and the filter which transmits only the third harmonics. Since the amplitude of the third harmonics is small, we amplify it by the variable-gain amplifier. The amplitude of the third harmonics is set to 1/6 of that of the fundamental wave, and when its phase is so adjusted that it is out of phase with respect to the phase of the fundamental wave at  $\theta = 0$ , we obtain the synthesized waveform shown in Fig. 2b. To keep this waveform, parallel resonators with resonance frequencies  $f_0$  and  $3f_0$  are connected to the drain. Bias voltage  $V_{GS}$  of the dual gate FET is adjusted so that it operates as a class A amplifier. The synthesized voltage which is the output of the dual gate FET is supplied to the gate of FET1 through a coupling capacitance  $C$ . As shown in Fig. 4, we need only a part of synthesized waveform, namely, we

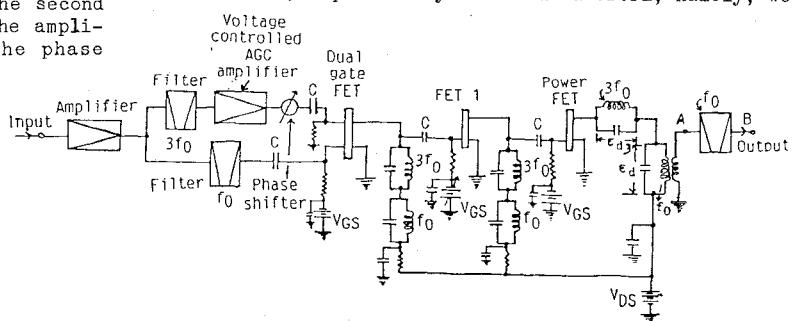


Fig. 3 Circuit constitution of the high efficiency single power amplifier

need the waveform which exists above the line corresponding to the operating angle  $74^\circ$ . Hence we adjust the bias voltage  $V_{GS}$  of FET1 so that it gives the operating angle  $74^\circ$ . But, since it is difficult to set the bias voltage accurately, the author adjusted  $V_{GS}$  by observing the synthesized waveform at the drain of FET1 using a sampling oscilloscope.

When we amplify the synthesized voltage by FET1, we obtain the waveform that is closest to a square wave at the terminals of parallel resonators with resonance frequencies  $f_0$  and  $3f_0$ . If we use only the resonator with resonance frequency  $f_0$ , the load impedance becomes much smaller than the resonance impedance for the voltage of the third harmonics and the harmonic component in the voltage appearing the load becomes much smaller than the fundamental component. Hence the waveform across the load is regarded as the waveform of the fundamental wave and we cannot obtain the synthesized waveform shown in Fig. 2b. To obtain this waveform, we need the parallel resonator with resonance frequency  $3f_0$ . Hence we employ, in the circuit system of Fig. 3,

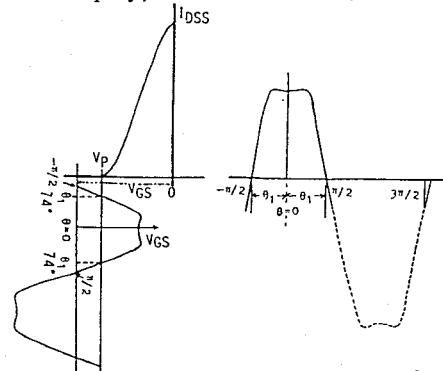


Fig. 4. Bias voltage for obtaining the synthesized voltage whose operating angle is  $74^\circ$ .

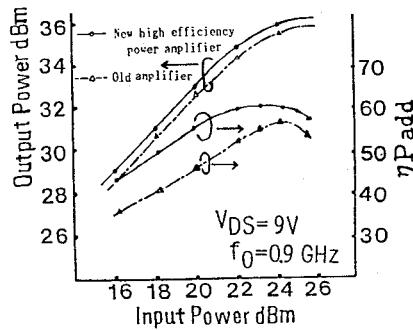


Fig. 5. Dependence of the output power and the power added efficiency on the input power for the amplifier of Fig. 3.

the two resonators with the resonance frequencies  $f_0$  and  $3f_0$  which are connected in series.

If we supply, through a coupling capacitance  $C$ , the waveform that is closest to a square wave to the gate of a power amplifying FET at the final stage, the period in which the drain voltage is low becomes longer and the drain current flows in this period. Hence we have the high efficiency amplifier.

The resonance frequencies  $f_0$  and  $3f_0$  of the resonators in Fig. 3 are 0.9 and 2.7 GHz, respectively. If we construct these resonators by lumped-constants circuits, we cannot obtain large  $Q_L$  owing to the skin effect. On the other hand, if we construct them by distributed-constant circuits, the wavelength is long and the volumes of them are large. Hence also in this case it is difficult to obtain large  $Q_L$  on account of the skin effect. In constructing the high efficiency amplifier, not only high efficiency but also large output power are required. In order to obtain such an

amplifier, we need resonators having large  $Q_L$  for the frequencies  $f_0$  and  $3f_0$ . The author replaced the resonators of  $f_0$  and  $3f_0$  by coaxial dielectric resonators and constructed a high efficiency amplifier. The bandwidth of the parallel resonator for the frequency  $f_0$  is 40 MHz and  $Q_L = 24$ .

The voltage  $V_{DS}$  applied between the drain and source of the power amplifying FET is 9 V, the bias voltage  $V_{GS}$  is -3.2 V. This bias voltage corresponds to the cutoff voltage  $V_p$  in Fig. 5. Under these conditions, the FET operates as a class B amplifier.

When the input power was fixed to 22 dBm and the frequency was varied from 0.8 to 1.1 GHz, we obtained the output power 35 dBm(3.3 W), the bandwidth 40 MHz, and the power added efficiency 60 %. Figure 5 shows the characteristic curves of the output power and power added efficiency. When the frequency was fixed to 0.9 GHz and the input power was varied from 16 to 26 dBm, the output power changed from 29 to 36.1 dBm and the power added efficiency changed from 44 to 60 %.

When the circuit system of Fig. 3 was used, the power added efficiency did not take its maximum at the input power which yielded the maximum output power. The maximum efficiency 60 % was obtained the input power of 22 dBm.

If we cutoff the output of the variable-gain amplifier in Fig. 3, we have only the fundamental wave. In this case, when we increase the amplitude of the input voltage applied to the gate of FET1, we obtain in the drain the voltage which saturates at its maximum. When we apply this voltage to the gate of the final stage, the circuit system operates as a high efficiency amplifier, but if we want to increase the efficiency by using the waveform of Fig. 2b, we set the voltage decrease  $E_d3$  and  $E_d$  to 1/6 and 1, respectively, by adjusting  $Q_L$  of the parallel resonators with the resonance frequencies  $f_0$  and  $3f_0$ . Although we know that the amplitude ratio between the voltages with  $f_0$  and  $3f_0$  can be varied by changing  $Q_L$ , it is difficult to carry

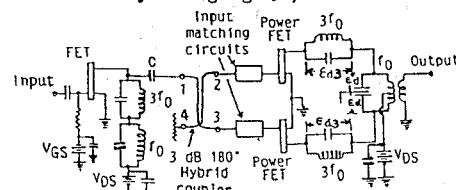


Fig. 6. Circuit constitution of a high efficiency push-pull power amplifier represented by lumped-constant elements.

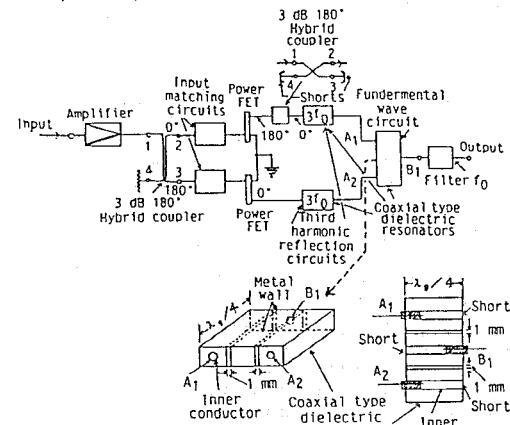


Fig. 7. High efficiency of a high efficiency push-pull power amplifier.

out this adjustment for the resonators composed by the distributed-constant circuit. Hence, when we use the voltage waveform saturating at its maximum, we obtain

at the drain of the final stage merely the synthesized voltage waveform which is close to a square wave but has unknown radio between the voltages with  $f_0$  and  $3f_0$ . The dash-dot curves in Fig. 5 show the measured output power and power added efficiency as functions of the input power obtained in a case that the synthesized voltage mentioned above was used. As seen from the curves, the maximum output power is 35.8 dBm and the power added efficiency is 56 %. From the above discussion, it is clear that, when we employ the simplified circuit system in which the output power of variable-gain amplifier is cutoff, the output power and the power added efficiency are lower than those obtained by the high efficiency amplifier of Fig. 3. To solve this problem, the author devised the circuit system of Fig. 3 and, by the experiment, confirmed that the output power and the power added efficiency are large.

## 2.2 High Efficiency Push-Pull Power Amplifier

Figure 6 shows the circuit structure of a high efficiency push-pull amplifier. In Fig. 6, the resonator with  $f_0$  is for picking up the fundamental wave, and the filter with  $3f_0$  is for reflecting the third harmonics. We replace the lumped-constant circuits with coaxial-type dielectric resonators, and the resulting circuit is shown in Fig. 7. The electrical lengths of these distributed-constant circuits are all  $\lambda/4$  as shown in Fig. 7.

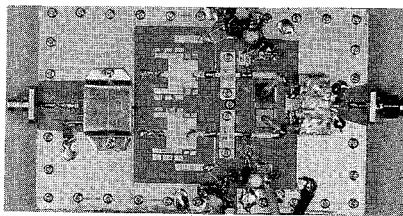


Fig. 8. Photograph of the high efficiency push-pull power amplifier shown in Fig. 7

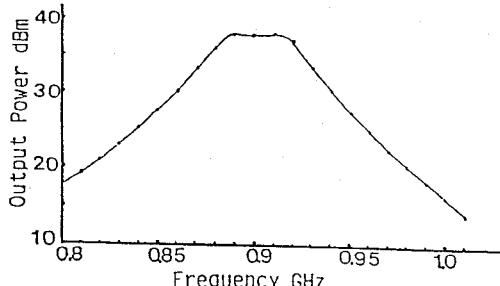


Fig. 9. Frequency characteristics of the high efficiency push-pull power amplifier shown in Fig. 8.

Fig. 8 is a photograph of the push-pull power amplifier shown in Fig. 7.

The bias voltage  $V_{ds}$  across the drain and source of the two power FETs is 9 V, and the bias voltage  $V_{gs}$  across the gate and source is -3.2 V which is on the cutoff point  $V_p$  of the FET. By adopting these bias voltages, the circuit system of Fig. 7 works as a class B push-pull power amplifier.

Figure 9 shows the frequency characteristics which was obtained when the input power was constant 25.6 dBm(370 mW) and the frequency was changed from 0.8 to 1.1 GHz. The output power was 39 dBm(8 W), the bandwidth was 450 MHz, and the power added efficiency of 81 % was obtained.

Figure 10 shows the characteristic curves of the input power versus output power and of the power added efficiency. When the frequency is constant 0.9 GHz and

the input power was changed from 17 to 29 dBm, the output power varied from 36 to 39 dBm and the power added

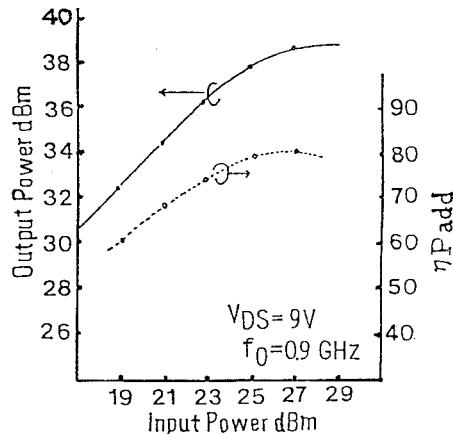


Fig. 10. Dependence of the output power and the power added efficiency on the input power for the amplifier of Fig. 8.

efficiency varied from 58 to 81 %.

## IV CONCLUSION

We have described the high efficiency class B single and push-pull power amplifiers. The most important point in constructing the high efficiency power amplifier is that, when the voltage amplitude of the fundamental wave is unity, the amplitude of the third harmonics should be 1/6 or 1/7 and the waveform of the third harmonics should be out of phase relative to the fundamental wave at  $\theta = 0$ . It was confirmed from the experiment that, if we set the operating angle of the synthesized voltage to a value in the range  $70^\circ - 74^\circ$ , we obtain the waveform that is closest to the square wave and this waveform is the most desirable one for constructing the high efficiency amplifier. Although it is important to make the efficiency higher, it is also important to make the output power larger. To obtain the large output power, we should use the parallel resonators for  $f_0$  and  $3f_0$  which have large  $Q_L$ . This point was confirmed by the experiment. The circuit systems for the high efficiency amplifiers using the waveforms of Figs. 2d and 2e have also been described in this paper.

## REFERENCES

- 1) D. M. Sinder, "A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdrive RF Power Amplifier," IEEE Trans., Vol. ED-14, No. 12 Dec. 1967.
- 2) K. Chiba, "GaAs FET Power Amplifier Module with High Efficiency," Electron. Lett. Vol. 19, No. 24, PP. 1025-1026, Nov. 1983.
- 3) B. D. Geller and P. E. Goettle, "Quasi-Monolithic 4 GHz Power Amplifier with 65 Percent Power Added Efficiency," IEEE, MTT-s Digest, PP. 835-838, 1988.
- 4) Sachihiko TOYODA "Broad-Band Push-Pull Power Amplifier," IEEE, MTT-s Digest, PP. 507-510, 1990.